Physical Design Engineer Resume Samples

4.8 (101 votes) for Physical Design Engineer Resume Samples

THE GUIDE TO RESUME TAILORING

Guide the recruiter to the conclusion that you are the best candidate for the **physical design engineer** job. It's actually very simple. Tailor your resume by picking relevant responsibilities from the examples below and then add your accomplishments. This way, you can position yourself in the best way to get hired.

- Craft your perfect resume by picking job responsibilities written by professional recruiters
- Pick from the thousands of curated **job responsibilities (/job-descriptions/physical-design-engineer)** used by the leading companies
- Tailor your resume & **cover letter (/cover-letters/physical-design-engineer)** with wording that best fits for each job you apply

Brett Williamson

8367 Anibal Flat, Chicago, IL • Phone: +1 (555) 279 3424

EXPERIENCE

MAYER INC
Philadelphia, PA

- Will be responsible for all aspects of Physical Design for Full chip/Blocks covering floorplanning, budgeting, Clock Trees timing & analysis, Placement, Scan re-ordering, Clock tree synthesis, Placement optimizations, Routing, Timing and SI analysis/closure, ECO tasks (both timing and functional), EM/IR, DRC, LVS, ERC analysis & fixes, Low Power solution development & implementation
- Be a highly-valued member of our start-up like team through excellent collaboration and teamwork with other physical design engineers as well as with the RTL design team
- Your work will focus on the full development flow: Floor planning, Bus / Pin Planning, Clock Tree Synthesis, Placement, Optimization, Routing, Parasitic Extraction, Static Timing Analysis, IR drop analysis, Physical Verification and Sign Off
- Responsible for Physical Implementation of an IP - starting from Netlist to GDS, including floorplanning, Placement, Clock design, Optimization, Timing closure, DRC/LVS, LEC, MVRC and sign off
- Knowledge with Chip Level Floor planning, Bus / Pin Planning, Clock Tree Synthesis, Placement, Optimization, Routing, Parasitic Extraction, Static Timing Analysis, IR drop analysis, Physical Verification and Sign Off will be helpful
- Effective communicator to provide status of the progress, problem and solution to management and other engineers
- Participate in developing methodologies, flow automation and improvements on existing flows to increase productivity

HELLER INC
Dallas, TX

- Leading and mentoring junior employees and interfacing with front end design team to improve RTL and design quality
- Implement/Support blocks with multi-voltage designs through all aspects of RTL to GDS Implementation (Place and Route, static timing, physical verification) using industry standard EDA tools
- Running/supporting/maintaining the Global Assembly Flow using industry standard EDA tools for designing the next generation Multi-Ghz high-performance processor SOC chips in leading-edge CMOS process technology
- Physical design knowledge, from netlist handoff to GDS tape out including floor planning, place and route, clock tree synthesis, timing closure and physical verification
- Expert in developing Synopsys ICC based flows to drive block PnR, Timing Closure and Final sign off
- Working knowledge of deep sub-micron issues
- Provide technical direction, coaching, and mentoring to employees on your team and others when necessary to achieve successful project outcomes

STEHR, JONES AND HIRTHE
Houston, TX
present

- Working knowledge of Extraction and STA methodology and tools
- Flow development to avail of latest enhancements in implementation tools
- Work with physical verification team to integrate these blocks seamlessly into full chip partitions
- Use metric-driven techniques to help ensure first-pass working silicon
- The individual is expected to be an expert in multiple aspects in PD areas and provide technically leadership to the engineering team
- Provide technical direction, coaching, and mentoring to employees on the team and others when necessary to achieve successful project outcomes
- Familiar with hierarchical design approach, top-down design, budgeting, timing and physical convergence

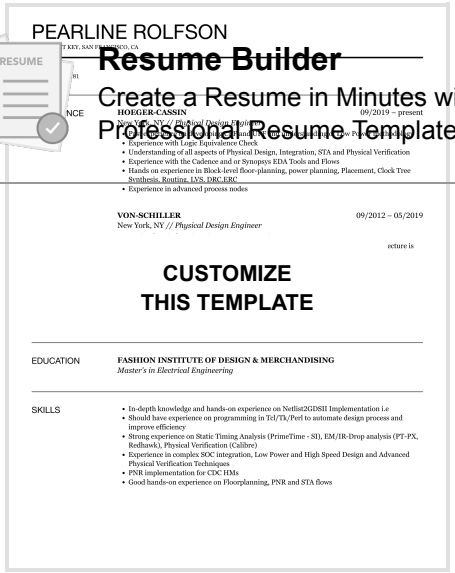
EDUCATION

ILLINOIS STATE UNIVERSITY
Bachelor's Degree in Electrical Engineering

SKILLS

- High problem solving capacity and good tolerance for ambiguity able to prioritize tasks independently
- Ability to work independently and develop quick engineering solutions for complex problems
- Excellent understanding and hands on experience with physical verification (DRC/LVS/ERC/antenna) and other reliability checks(IR/EM/Xtalk)
- Good knowledge of EDA tools from Synopsys, Cadence and Mentor, particularly with Encounter & Calibre
- Excellent analytical and problem solving skills along with attention to details
- Comprehensive knowledge to the complete digital P&R flow
- Able to run small mini projects with minimal supervision
- Experience with Synopsys EDA tools spanning the RTL to GDSII considered desirable but not essential
- Knowledge of Telcordia and/or military, IPC and ASME standards
- Knowledge of MCAD, Pro-E, CREO2

15 PHYSICAL DESIGN ENGINEER RESUME TEMPLATES



PEARLINE ROLFSON

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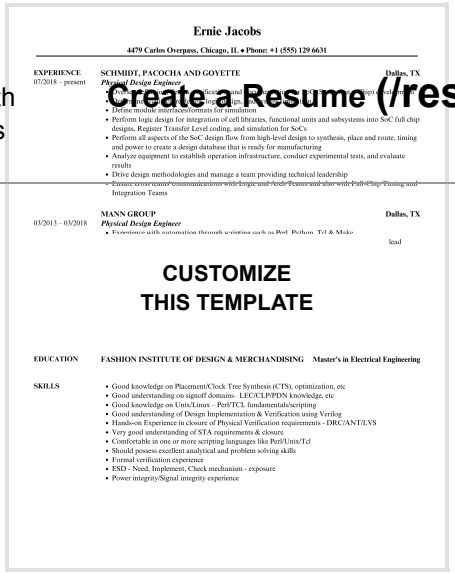

Ernie Jacobs

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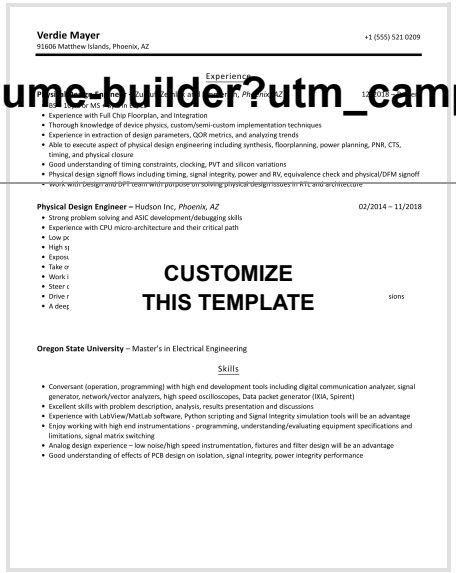

Verdie Mayer

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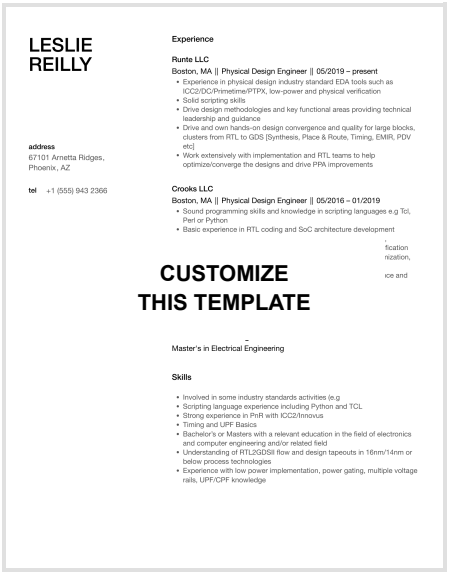

LESLIE REILLY

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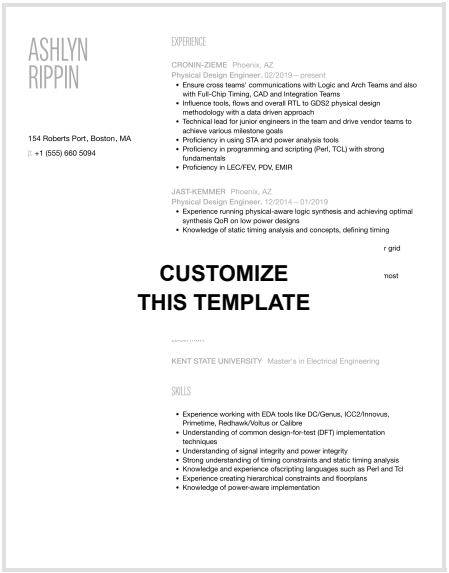

ASHLYN RIPPIN

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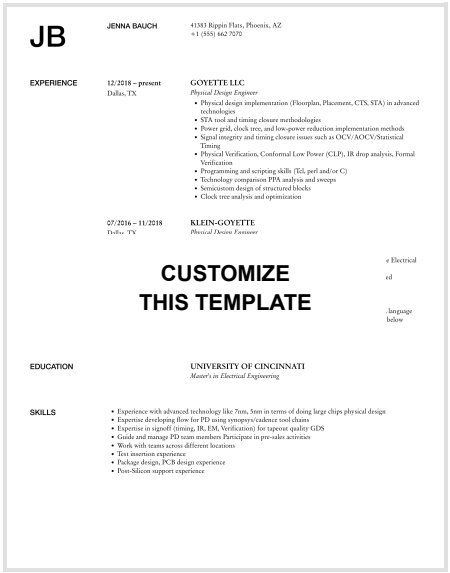

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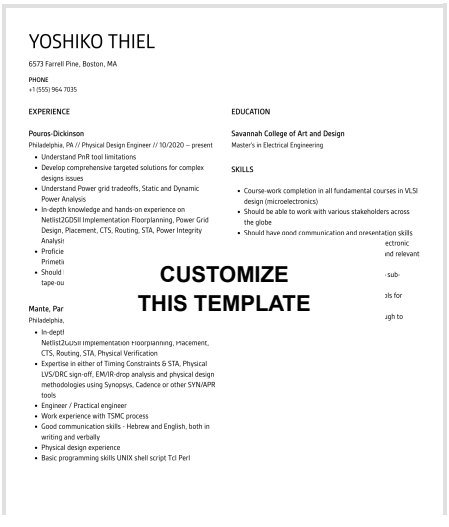

YOSHIKO THIEL

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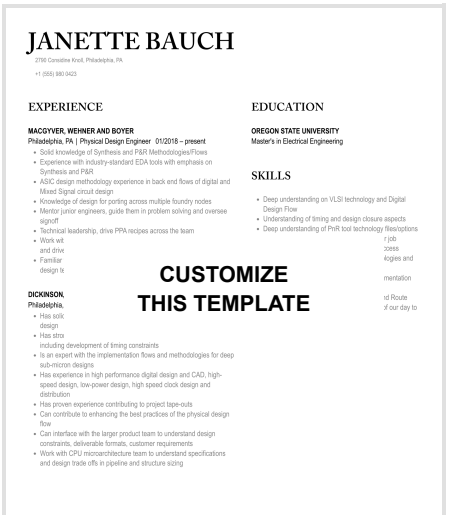

JANETTE BAUCH

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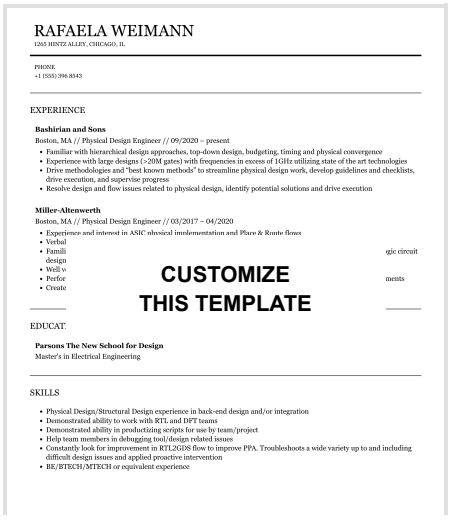

RAFAELA WEIMANN

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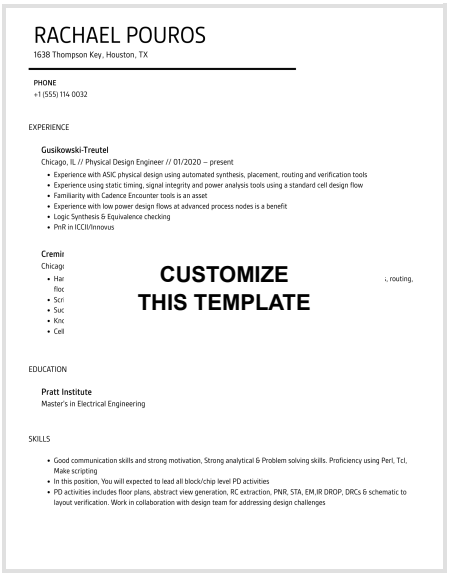

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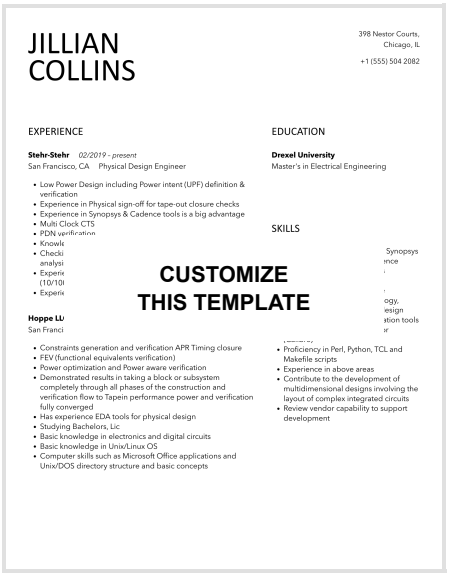

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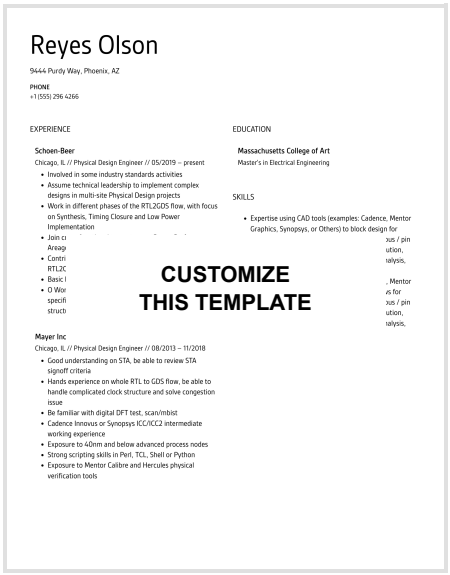

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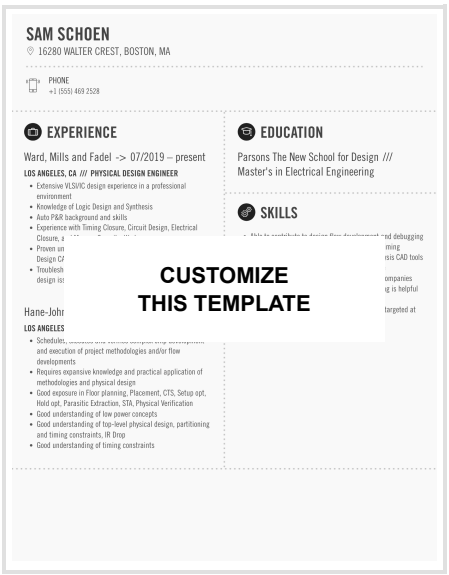

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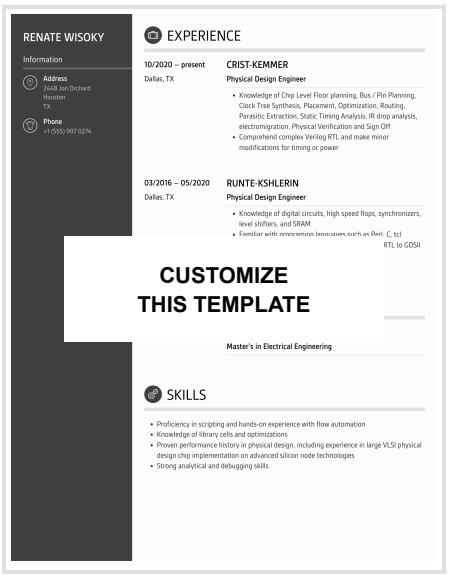

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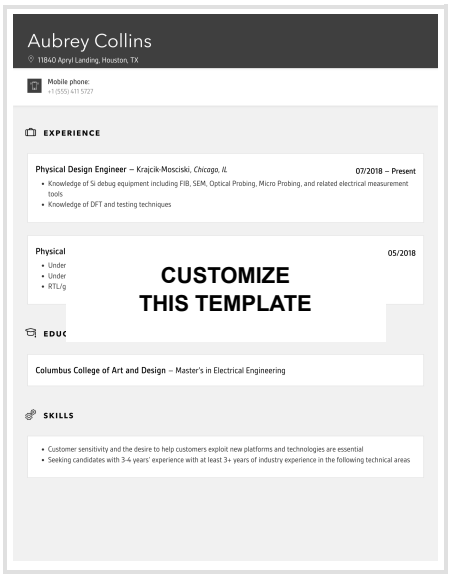

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How to Tailor Your Resume (https://www.velvetjobs.com/resume/tailor-your-resume)

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How to Mention Achievements (https://www.velvetjobs.com/resume/resume-accomplishments)

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What to Put on a Resume (https://www.velvetjobs.com/resume/what-to-put-on-a-resume)

How Long Should a Resume Be (https://www.velvetjobs.com/resume/how-long-should-a-resume-be)

The Best Resume Format (https://www.velvetjobs.com/resume/resume-formats)

How to List

CV vs.

Include

1 Physical Design Engineer

Resume Examples & Samples

- Understanding of standard cell architecture
- Design of standard cell layouts for newest process technologies
- Optimization of standard cell layouts considering area/performance/reliability trade-offs
- Verification of layouts for design and architecture rules
- Understanding and implementation of DFM and ESD guidelines
- Understanding of RC delay, electro migration, self-heating and coupling capacitance
- Ability to recognize failure prone layout structures and produce robust layouts
- Equivalence verification of layouts with respect to schematics
- Development of automation for library design, quality checking and reliability verification
- Exploration of standard cell library architecture with optimal placement and routing
- Release verification and hand-off
- You must possess a minimum of Bachelor's degree in Electronics Engineering
- VLSI/CMOS design certification/training
- Experience in VLSI layout mask design
- Experience using industry-standard layout tools for designing layouts and verification
- Experience in scripting development (TCL, Perl)

2 Physical Design Engineer

Resume Examples & Samples

- Self-starting, creative thinking, and open attitude

- BS or MS in computer science/engineering or electrical engineering
- Minimum of 3 months experience with Verilog design languages to target technologies via synthesis, place, and routing tools
- Minimum of 3 months experience of Verilog, Unix environment, TCL/TK programming language

3 CPU Physical Design Engineer

Resume Examples & Samples

- Experienced in Synthesis, APR and Timing tools and flows
- Perl and TCL coding
- 3-10 years experience with the above skill sets

4 FIP Physical Design Engineer

Resume Examples & Samples

- Working experience in circuit & layout design, through verification on advanced technology nodes using Industry standard design tools
- Experience ranging from leaf level cell design to chip level integration desired
- Working knowledge of UNIX with preferred skills in scripting for data conversion
- Foundation in analog constraint specification and capture
- Foundation in best layout practices for analog circuit layouts
- Foundation and experience in automated layout practices, layout views for SOC designs
- Excellent working ability with circuit design and layout methodologies in a team environment

5 Central Processing Unit Physical Design Engineer

Resume Examples & Samples

- Employing physical design construction, analysis, automation and verification tools to deliver completed section, unit or sub-system designs for inclusion in full-chip SOCs
- Integrating IPs to deliver completed SOC designs
- Providing IP integration support to SOC customers
- Participating in the development of architecture and micro-architecture specifications for various components
- Performing logic design and Register Transfer Level (RTL) coding, simulation and verification
- Bachelor's or Master's Degree in Electrical or Computer Engineering

- Minimum 3 months experience with CMOS transistor level circuit fundamentals, hardware design, and programming
- Experience in designing high-speed, low-power digital circuits, floorplanning, timing convergence, physical design convergence, formal equivalency verification, device layout, and design rule checking
- Familiarity with logic synthesis and automated place and route tools
- Strong background in computer architecture and logic design fundamentals
- Exceptional scripting skills using a programming language such as Perl, TCL, or Python

6 Asic / SOC Physical Design Engineer

Resume Examples & Samples

- Logic synthesis of design blocks
- Formal/Logical Equivalence Verification (FEV)
- Circuit simulation of critical path elements
- Physical verification - Layout vs. Schematic (LVS), Design Rule Checks (DRC), Electrical Rule Checks (ERC), and Design for Manufacturability checks (DFM)
- BS degree in Electrical or Computer Engineering
- Completed coursework or one or more classroom projects using C, C++, PERL, Python, or TCL programming
- Completed coursework or one or more classroom projects to demonstrate understanding of CMOS transistor-level circuit design fundamentals

7 Structural Physical Design Engineer

Resume Examples & Samples

- Floorplanning
- Auto Place and Route
- Static Timing Analysis and Closure
- Functional Equivalence Verification
- Full Chip Layout Verification
- Reliability Verification
- Ability to work independently and work at various levels of abstraction
- Ability to code in Perl and TCL

- Able to work in a dynamic and team oriented environment
- Digital VLSI design
- Programming with C++, Perl, TCL, and/or Python
- CAD algorithms in the physical design space
- Standard cell creation and characterization

9 Physical Design Engineer

Resume Examples & Samples

- Degree in Electrical Engineering or Information Technology required
- Main focus on Microelectronics desired
- 5 years or more of relevant work experience is required
- Programming skills desired
- Unix skills required
- Experience with Place & Route of state of the art designs using deep submicron technologies required or FinFET technology is desired
- Knowledge of Synopsys Backend Design Flow required
- English Language skills required & French Language skills desired

10 Physical Design Engineer

Resume Examples & Samples

- Confidently represent MD team in key project meetings/events
- 2 Years experiences in outstanding leadership, communication and influencing skills
- Demonstrate Solid understanding of basic electronic circuit functionality and behaviors
- 2 years Advanced debug of CAD tool & utility issues
- Ability to work well in a team environment

11 ICE Physical Design Engineer

Resume Examples & Samples

- B.TEch/M.Tech in VLSI/Electrical/Electronics Engineering

- Experience in digial and analog layout design
- Basic understanding of VLSI design

12 Senior Physical Design Engineer

Resume Examples & Samples

- BS/MS in EE/CS and
- 4+ years of experience physical design methodologies and sub-micron technology
- 3+ years of experience with place&route, physical verification (DRC/LVS/Antenna)
- 3+ years of experience programming in Tcl/Tk/Perl to automate design process and improve efficiency
- 4+ years of experience with Synopsys suite (IC Compiler, Primetime, Design Compiler, IC Verifier)
- 4+ years of experience in static timing analysis (PrimeTime), EM/IR-Drop/Xtalk analysis (PT-SI, Apache), formal or physical verification (Formality, Verplex, IC Verification, Calibre)
- 4+ years of experience in the practical application of methodologies and physical design tools, flow automations and improvements
- 3+ years of experience in complex SOC integrations, low power and high speed design, advanced verification techniques

13 Physical Design Engineer

Resume Examples & Samples

- Chip and block level floor planning, analysis of floor plan options taking into account timing and area budgets
- Net list generation, including synthesis, constraints, timing analysis and equivalence checking
- Place and route, timing closure and power analysis
- Comprehensive knowledge to the complete digital P&R flow
- Experience in logic synthesis, constraints and STA/PTSI
- Experience in chip/block level floor planning and P&R
- Experience in CTS and timing closure
- Experience of power planning, power sign-off and IR Drop Analysis
- Experience in crosstalk noise analysis, physical verification, LVS and DRC
- Experience in DFT, MBIST, scan, coverage
- Experience with Synopsys EDA tools spanning the RTL to GDSII considered desirable but not essential
- Broad software skills including Perl, Tcl, Unix and Linux

14 Senior Physical Design Engineer

Resume Examples & Samples

- 6+ years of experience physical design methodologies and sub-micron technology
- 6+ years of experience with place&route, physical verification (DRC/LVS/Antenna)
- 6+ years of experience programming in Tcl/Tk/Perl to automate design process and improve efficiency
- 6+ years of experience with Synopsys suite (IC Compiler, Primetime, Design Compiler, IC Verifier)
- 6+ years of experience in static timing analysis (PrimeTime), EM/IR-Drop/Xtalk analysis (PT-SI, Apache), formal or physical verification (Formality, Verplex, IC Verification, Calibre)
- 6+ years of experience in the practical application of methodologies and physical design tools, flow automations and improvements
- 6+ years of experience in complex SOC integrations, low power and high speed design, advanced verification techniques
- Self-motivated team worker, good verbal and written communication skills
- Experience in synthesis, timing closure
- Working knowledge of DFx techniques and tools
- Experience on high speed processor design

Physical Design Engineer

Resume Examples & Samples

- Must have a BS or MS in Electrical Engineering , Computer Engineering, Computer Science
- Must have the unrestricted right to work in the US without requiring sponsorship at the BS level only
- Three months coursework or experience in at least 2 of the following areas
- Internship with high tech company
- Experience with Synopsys tool suite (DC, ICC, Primetime)
- Experience with Schematic entry and layout visualization using Cadence or Synopsys tools
- Experience with low-power VLSI design techniques
- Experience with Design for test, debug and manufacturing

16

Physical Design Engineer

Resume Examples & Samples

- Understand latest (16nm/14nm) technologies, work with CAD/Guidelines team of changes needed suitable for design closure
- Responsible for Physical Implementation of an IP - starting from Netlist to GDS, including floorplanning, Placement, Clock design, Optimization, Timing closure, DRC/LVS, LEC, MVRC and sign off
- Work closely with a global team to root cause Physical Implementation issues related to design/tools etc. and arrive at a feasible solution
- Crisp written and Oral communication with global teams
- Hands On experience with SNPS, Mentor and Cadence tools, ICC, PrimeTime, Design Compiler, Calibre DRC/LVS experience a must
- Automation using PERL, TCL, Python is a MUST
- Must have taped out Multi-Billion transistor hierarchical designs - recent experience

17

Serdes Phy-physical Design Engineer

Resume Examples & Samples

- 10+ years of overall design experience, preferably with high speed multi-gigabit SerDes PHY designs or other high performance IP designs
- Experience in automated synthesis and timing driven place and route of RTL blocks (Verilog experience preferred) for high speed datapath and control logic applications
- Strong background in digital circuit techniques, efficient and robust implementation topologies for

logic functions, logic optimization, and transistor level circuit topologies for high speed, low power applications

- Experience in floorplanning, establishing design methodology, IP integration, checks for logic equivalence, physical/timing/electrical quality, and final signoff for large IP delivery
- Versatility with scripts to automate design flow, simulation test benches, and quality checks

18 Senior Physical Design Engineer

Resume Examples & Samples

- MSEE with 5+ years or Bachelor with 7+ years of industrial experience in ASIC design
- Plus if good programming skill on caliber design rule
- Experienced in Calibre usage, DRC/LVS debug and chip Tapeout
- Good listening, writing and speaking English, and need frequently involve global teams meeting on new process update
- LI-MZ1

19 Senior Physical Design Engineer

Resume Examples & Samples

- GNB FCT, Work with global Front-End design team and physical design team for large scale ASIC chip physical implementation. Focus on physical design of deep sub-micron GPU chips including block level (full chip) floor planning and timing closure
- The individual is expected to be an expert in multiple aspects in PD areas and provide technically leadership to the engineering team
- The individual is also expected to be accountable for project delivery
- Familiar with Back-End (physical design) EDA tools and P&R flow

20 Microprocessor Physical Design Engineer

Resume Examples & Samples

- Individual will be responsible for performing Physical Design activities for POWER & System Z microprocessors and subsystems
- Responsibilities includes Block-level timing closure of high frequency designs (4GHz+) such as Processor Core, Cache Controllers, interfaces like PCIe and IBM proprietary bus architectures. Includes design planning, synthesis, placement & route and critical sign-off checks to achieve required Quality of Result
- PhD/Master's/ Bachelor's Degree in Engineering

- Skills :Physical design of server processor. You should have proven skill in floor planning, synthesis, Placement & Routing, physical design verification and other sign-off checks, timing analysis and closure. Server physical design and statistical timing experience will be a plus
- At least 7 years experience in Physical Design of Server Processor
- At least 7 years experience in Synthesis, Placement, Route, floorplaning, timing analysis, PDV cleanup

21 Physical Design Engineer

Resume Examples & Samples

- 8 years' relevant work experience including 3+ Experience in ASIC Design with relevant Physical Design Skills preferred
- Minimum BSEE/CE, or equivalent degree, Masters is definitely as asset
- Must be a self-starter, and able to independently and efficiently drive tasks to completion
- Ability to provide mentorship and guidance to junior engineers and be a very effective team player

22 Physical Design Engineer Lead

Resume Examples & Samples

- Have an in depth understanding and experience for all Physical Design activities for a large, leading technology SOC ASIC chip
- Great team player able to effectively interact and collaborate with other Physical Design Engineers and drive resolution of all Physical Design related issues
- Knowledge with Chip Level Floor planning, Bus / Pin Planning, Clock Tree Synthesis, Placement, Optimization, Routing, Parasitic Extraction, Static Timing Analysis, IR drop analysis, Physical Verification and Sign Off will be helpful
- Strong communication, Time Management and Presentation Skills
- Forward looking, capable of working as an independent contributor who proactively identifies and resolves issues / roadblocks before they become bottleneck / showstopper
- Ability to provide mentorship and guidance to junior and senior engineers and be a very effective team player

23 Senior Physical Design Engineer

Resume Examples & Samples

- 5+ years of experience in physical design, tapeout experience in 28nm or advanced process is a plus

- Knowledgeable in all aspects of ASIC design flow
- Familiar with Front-End tools and RTL is a plus
- Good at scripts, like Python/Tcl

24 Synthesis / APR Physical Design Engineer

Resume Examples & Samples

- Debugging post-silicon circuit issues
- Back-end physical design
- Ability to be flexible between multiple roles throughout the life of the project
- Synopsis design and verification tools
- Synthesis tools like Design Compiler
- APR (auto place & route) tools like ICC/Astro
- Static timing tools like PrimeTime
- Proficient in scripting (PERL and/or TCL)

25 SOC Physical Design Engineer

Resume Examples & Samples

- High motivation with a strong work ethic
- Good planning skills
- Bachelor of Science degree in Electronics Engineering or Computer Engineering
- 6 months experience with physical layout
- 6 months experience in digital or mixed signal design
- Good understanding of RTL-based (Verilog or VHDL) design methodology
- 1 year working knowledge of Linux OS and scripting languages (e.g. TCL, Perl
- Experience with signal routing
- Experience with clock tree synthesis
- Experience with design for test
- Experience with signal integrity and noise analysis
- Experience with low-power design techniques or timing analysis

26 Physical Design Engineer

Resume Examples & Samples

- Bachelor's Degree in Electrical/Hardware and/or Computer Engineering or Bachelor's Degree in Mechanical/Hardware and/or Computer Engineering
- Previous internship experience in CPU or SOC physical design
- Experience with VLSI circuits, design techniques, and sub-micron CMOS technologies
- Experience in designing high-speed, analog circuits, floor planning, timing convergence, physical design convergence, formal equivalency verification, device layout, and design rule checking
- Familiarity with hardware description languages such as Verilog or System Verilog
- Extensive scripting skills using a programming language such as Perl, TCL, or Python

27 Physical Design Engineer

Resume Examples & Samples

- B.Sc. in EE or equivalent
- Requires 4-6 years of experience in RTL to GDSII implementation and verification of digital macros preferable in synopsys DC/ICC implementation tools as well as static timing and Formal verification
- Scripting capabilities in tcl, perl

28 RF IC Physical Design Engineer

Resume Examples & Samples

- Must have a BS, MS or PhD in Electrical Engineering, Computer Engineering or related discipline or in lieu of a degree, a minimum of 7 years of RFIC circuit physical design experience
- Minimum 5 years of radio-frequency integrated circuit physical design experience including experience in both Cadence design flow and Intel's Genesis tool
- Experience with foundry technology in 65nm and 28nm nodes
- Knowledge of layout of inductors, transformers and other passive devices
- Must understand how to run extraction tools and how to use that feedback to guide physical design
- Experience with Intel's advanced technology nodes

29 Physical Design Engineer

Resume Examples & Samples

- Bachelors or Masters of Engineering degree in the relevant fields with 3+ years of experience in ASIC/Physical design area

- A wide breadth of layout knowledge is required
- Ability to program in C/C++ is a plus
- In depth understanding of product development on leading edge process technologies with a strong preference for hands on experience with Intel process technologies

30 Physical Design Engineer Manycore Processors

Resume Examples & Samples

- BSEE/MSEE with minimum of 10 years in VLSI Design
- Needs to be familiar with all aspects of ASIC integration including floorplanning, clock and power distribution, global signal planning, I/O planning and hard IP integration
- Experience solving SoC issues such as multiple voltage and clock domains, ESD strategies, mixed signal block integration, and package interactions
- Must have experience on integrating IP from both internal and external vendors and be able to specify and drive IP requirements in the physical domain
- Experience with large SoC designs (>20M gates) with frequencies in excess of 1GHz utilizing 28nm and more advanced technologies
- From a CAD tool perspective, experience with floorplanning tools, P&R flows, global timing verification and physical design verification flows is required
- TCL and Perl mastery are a necessity; Make and Python expertise is nice to have

31 Backend / Physical Design Engineer

Resume Examples & Samples

- B.Sc. in Computer Engineering/ Electronic Engineering from a leading university
- 0-15 years of experience in P&R tools, expertise in Netlist-to-GDSII flow
- Experience in unit and top level floor planning
- Team player, responsible and motivated

32 Physical Design Engineer AS

Resume Examples & Samples

- Involved in all aspects of physical implementation from RTL to GDS
- Perform RTL synthesis and scan stitching
- Create timing constraints
- Analyze power constraints and chip floor plan

- Analyze clock distribution on full chip assembly
- Develop Placement & Route
- Create Static Timing Analysis, timing closure, ECO and tape-out
- IR Drop analysis
- Bachelor's or Master's in Electrical Engineering and 4+ years of industry experience in a Logic design or Physical Design position
- Candidate should have strong knowledge of RTL design and must be familiar with RTL compiler/Design Compiler, ICC/SOC Encounter
- Candidate should have Primetime, Conformal LEC, and ATPG
- Candidate will also have working knowledge of scan insertion, and ATPG
- Must have good communication and teamwork skills
- Be able to participate in design/architecture reviews
- Define physical design methodologies and flow automation
- Ability to perform debug/analysis skills for designs, library and technology files

33 Physical Design Engineer Principal / Manager

Resume Examples & Samples

- Candidate should have exposure to chip power planning, bump and package planning
- Along with partitioning, candidate should have hands-on experience in Chip/block floor planning, placement optimizations, CTS and routing
- Excellent understanding and hands on experience with physical verification (DRC/LVS /ERC/antenna) and other reliability checks(IR/EM/Xtalk)
- Hands-on experience in Full chip level signoff STA
- Being proficient in TCL, Perl scripting is a plus
- B. Tech. / M. Tech. with 12-15 years of experience in Physical Design

34 Physical Design Engineer

Resume Examples & Samples

- Should have handled Netlist to GDS II at Chip/block level for multiple tape outs
- Hands-on expertise with technology nodes like 28nm, 16nm and below
- Good knowledge of EDA tools from Synopsys, Cadence and Mentor, particularly with Encounter & Calibre
- Hands-on experience in block/top level signoff STA
- Exposure in physical implementation of timing/functional ECO’s

- B. Tech. / M. Tech. with 7-10 years of experience in Physical Design

35 ~~Physical Design Engineer~~

Resume Examples & Samples

- Proficiency in multiple levels of layout design and verification using ICC
- Ability to comprehend issues of RC delay, electro-migration, self-heating, and cross capacitance
- TCL scripting would be added advantage

36 CPU Physical Design Engineer

Resume Examples & Samples

- Synthesis and APR (Design Compiler/ICC)
- Primetime, PTSI, Conformal LEC, RedHawk
- 3+ years experience with the above skill sets

37 Senior Physical Design Engineer

Resume Examples & Samples

- Have a solid background in circuits, electronics & physics & should be very willing to learn new technology for advance node and design methodology
- Skilled in scripting language, such as Perl, C shell, Makefile
- Feeling responsible for technical delivery, good team played, design quality/schedule focus

38 Physical Design Engineer

Resume Examples & Samples

- BSc degree in Computer Engineering/BS Computer science/Electrical Engineering
- 2+ years of experience in Digital Layout Designer
- Experience in block level and full-chip floorplan and implementation
- Understanding physical and electrical aspects of the technology
- Experience in configuring and running physical verification runsets (Calibre/ICV) on block level and on full-chip level
- Manipulations on GDS layers / mapping file

- DDR/GPIO ring implementation

39 **Physical Design Engineer**
Resume Examples & Samples

- 10+ Years experience with Multiple Fullchip Tape-in/Tape-out
- Knowledge on IP/Product Layout Quality
- Hands on Analog, IO, Custom and Semicustom Layout design
- Hands on Layout verification, Layout automation and Scripting language
- Experience in leading technically a small team of layout designers
- Work experience with external and/or internal key stake holders
- Teamwork, communication (vertical and/or horizontal) and problem solving skills

40 **Physical Design Engineer**
Resume Examples & Samples

- Independently assess and drive complex digital physical design assignments
- Work interactively and proactively with our CAD team to debug tool functionality and bugs
- Build and verify all levels of physical design hierarchy (leaf cell, IP block, compiler)
- Collaborate closely with SoC projects at various sites across Intel
- Bachelor’s Degree in Electrical Engineering, Computer Engineering, Computer Science or Technical educational background
- Minimum 3 years’ previous experience designing SRAM and/or RF compilers
- Proficient Programming skills (UNIX shell script, Tcl, Perl)
- Master’s Degree in Electrical Engineering, Computer Engineering or Computer Science

41 **Physical Design Engineer**
Resume Examples & Samples

- The ideal candidate will have 5+ years of Physical Design experience on high PHY and/or SOC designs
- Experience in developing and implementing Power-grid and Clock specifications
- Power user of industry standard Physical Design & Synthesis tools
- Solid Understanding of scripting languages such as Perl/Tcl
- Good understanding of Physical Design Verification methodology to debug LVS/DRC issues at

chip/block level

42 Physical Design Engineer

Resume Examples & Samples

- The ideal candidate will have 5-10 years of hands on experience in physical design and large chip integration
- Needs to be familiar with all aspects of ASIC integration including Floorplanning, Clock and Power distribution, global signal planning, I/O planning and hard IP integration
- Familiar with hierarchical design approach, top-down design, budgeting, timing and physical convergence
- Experience with large SoC designs (>20M gates) with frequencies in excess of 1GHz utilizing state of the art sub 45nm technologies
- A detailed understanding of database management issues will be required
- From a CAD tool perspective, experience with Floorplanning tools, P&R flows, global timing verification and Physical Design Verification Flows is required
- Familiar with various process related design issues including Design for Yield and Manufacturability, multi Vt strategies and thermal Mgt

43 Physical Design Engineer

Resume Examples & Samples

- The ideal candidate will have a minimum of 3-5 years of physical design experience, with recent successful tapeouts in deep submicron technology
- Expert in partition level P&R implementation, including floorplanning, clock & power distribution, timing closure, physical & electrical verification
- Strong knowledge of PD construction & analysis flows and methodology
- Proven ability to execute to stringent schedule & die size requirements
- Experienced in industry standard tools, understand their capabilities and underlying algorithms
- Experience with large SOC designs (>20M gates) with frequencies in excess of 1GHZ

44 Physical Design Engineer

Resume Examples & Samples

- 3-5 years experience in Physical Design
- Must have experience with taping out chips using 45nm or below

- Must have experience with the complete physical design flow using EDA tools Synopsys (PrimeTime, ICC is a must), Magma (Talus), Mentor Graphics (Caliber), and Cadence (First Encounter, Virtuoso, Conformal)

45 SOC Senior Physical Design Engineer

Resume Examples & Samples

- Perform circuit studies for low-power On-Die-Interconnect
- Investigate and evaluate asynchronous design options
- *This is an Intel Federal Position***
- Circuit design and feasibility
- Interconnect design and analysis

46 Physical Design Engineer

Resume Examples & Samples

- Must have strong Physical design skills, block level closure of all aspects , timing, cts, floorplaning etc
- Highly knowledgeable in solving technical challenges to achieve very low power , High Fmax closure
- 5-7 years of prior experience as a Physical Design Engineer

47 Lead Physical Design Engineer

Resume Examples & Samples

- Engineering, preferably in telecommunications
- Understanding of the Honolulu Authority for Rapid Transportation’s network infrastructure
- Resident in Honolulu to allow for a close collaboration of physical design and planning with the end customer
- Experience in Customer Management

48 Physical Design Engineer

Resume Examples & Samples

- Ability to work independently and develop quick engineering solutions for complex problems

- Ability to interface with engineers and managers by providing schedule updates and roadmap plans
- High problem solving capacity and good tolerance for ambiguity able to prioritize tasks independently
- Natural focus on quality, discipline, and accurate results for engineering customers. Experience in high-speed custom layout
- Proficient in floorplanning, RC extraction, layout optimization and verification
- Ability to contribute and work in a multi-site team setting
- Understanding of ESD, lithography, EM, DFM, antenna effects and manufacturing challenges
- Working knowledge of UNIX with experience in scripting and debugging-MS with previous analog layout experience
- High-speed custom layout
- Floorplanning, RC extraction, layout optimization and verification
- Working knowledge of UNIX with experience in scripting and debugging
- MS with previous analog layout experience

49 Physical Design Engineer

Resume Examples & Samples

- 6+ months of experience working with circuit design engineers and physical design team members in layout related tasks
- 6+ months of experience working in memory custom layout is a preferred qualification
- 6+ months of experience working with custom layout floor planning, RC extraction, layout optimization and verification
- 6+ months of experience working with ESD, lithography, EM, DFM, antenna effects and manufacturing challenges
- 6+ months of experience working with UNIX with experience in scripting and debugging
- 6+ months of experience working with VLSI circuits, design techniques, and sub-micron CMOS technologies
- 6+ months of experience working with designing high-speed, analog circuits, floor planning, timing convergence, physical design convergence, formal equivalency verification, device layout, and design rule checking
- 6+ months of experience working with logic synthesis and automated place and route tools
- 6+ months of experience working with hardware description languages such as Verilog or System Verilog

- Interacting with the RTL designers to correctly derive timing constraints, synthesize designs and evaluate timing optimizations
- Execute block level floor-planning, clock tree synthesis, place & route, timing closure at the block level
- Drive the block level's timing, DRC, LVS, FV convergence as well as participate in the convergence for full chip
- Participate in developing methodologies, flow automation and improvements on existing flows to increase productivity
- Help drive optimizations to SOC flows to improve the design efficiency and design quality
- Must have either a BS or MS in Electrical Engineering, Computer Engineering or Electrical and Computer Engineering
- Minimum 3 years of experience in VLSI design or ASIC/SOC design experiences including synthesis, floor-planning, clock tree synthesis (CTS), APR, static timing analysis, DRC/LVS, FV
- Knowledge of CMOS layout concepts
- Experience in UNIX operating system, scripting languages such as PERL, TCL, etc
- Experience with industry-standard IC CAD tools such as Synopsys DC, ICC and ICV based layout verification flows is desirable
- Circuit/physical design experiences in the high performance and ultra-low power IC designs is a plus

51 SOC Physical Design Engineer

Resume Examples & Samples

- Development of block-level constraints to drive synthesis, place and route, and timing verification
- Closure of timing, DRC, LVS, noise, electromigration, and other electrical rule sets
- Working with the microarchitecture team to define and document achievable power, performance, and area targets
- Assisting the design automation team by driving continuous improvements in all areas of physical design methodology
- Mentoring of less senior engineers in physical design and engineering best practices
- Seven or more years of experience in physical implementation of standard cell based designs from RTL to GDS
- Experience with synthesis, formal verification, auto-place and route, static timing analysis, and physical verification flows
- Strong communication skills and the ability to work with and influence a globally distributed team

- Familiarity with ARM or other embedded microprocessor based designs
- Familiarity AXI or other industry standard bus interface protocols
- Experience with peripheral IO protocols such as SPI, I2C, USB, Ethernet, etc
- Strong scripting ability in Perl, TCL, or Python

52 Digital Physical Design Engineer

Resume Examples & Samples

- BS in Electrical Engineering or related discipline
- 5+ years of experience in Physical Design
- 5+ years of experience in Digital Design of complex SoC IP Blocks and Products
- Experience in Digital Design and VLSI Fundamentals
- Knowledge in Physical Design of Chips, which includes VHDL, Verilog, C/System-C/System-Verilog/Specman
- Experience in Communication Systems Standards DSL, WLAN, Ethernet, Processor IP Cores MIPS, ARC, High-Speed Interfaces USB, PCIe, DDR, xGMII and ASIC Design Flow RTL to GDS
- Knowledge and expertise in Communication, Problem Solving and Documentation Skills
- Ability to work as part of a cross functional team in a dynamic environment

53 Physical Design Engineer

Resume Examples & Samples

- BSEE with 5 years or MS with 3 plus years of physical design experience including but not limited to RTL, Synthesis, Place and Route, Layout and integration into full chip
- Demonstrated knowledge of running performance analysis using STA as well as Spice level circuit analysis
- Strong working knowledge of STA. Understanding of developing complex clock constraints, false paths, noise, transient analysis using Primetime is essential
- Deep submicron technology background preferred

54 Senior Physical Design Engineer

Resume Examples & Samples

- Physical Implementation of high frequency cores Knowledge of CPU Architecture and Implementation concerns a plus
- Experience and knowledge of tools for physical design implementation (Floor planning, CTS,

P&R, STA) for CPUs and GPUs in advanced CMOS technologies STA tool and timing closure methodologies Power grid, clock tree, and low-power reduction implementation methods Signal integrity and timing closure issues such as OCV/AOCV/Statistical Timing

- Proficient in following tools and flows, DC, DCT, or DCG UPF Prime time
- Timing constraints capture in TCL CLP UPF Clock-domain-crossing
- It is also preferred if the candidate has RTL design experience with in-depth knowledge of low power design
- Familiar with Verilog and system Verilog

55 Senior Physical Design Engineer

Resume Examples & Samples

- This role encompasses responsibilities spanning early floor-planning, to tape-out, for cores and SoCs targeting NXP's Digital Networking portfolio, in the state-of-the-art deep sub-micron CMOS process technologies
- As part of the position the engineer will drive chip & high-frequency cores including- floor-planning, power grid design, placement, routing, signal integrity closure
- This engineer will work closely with logic designers and architects to optimize floor-plan for high performance cores, blocks and chip based on RTL and architectural input
- Minimum 7 years' experience
- Familiarity with either or both Cadence and Synopsys Physical design flows is a must
- Must have experience in floor-planning full chip – including partitioning chip into blocks, plan C4s, IO placement, verifying IR-drop, checking floor-plans for DRCs
- Previous experience floor-planning and building high performance ARM cores is a plus
- Must be able to place & route hierarchical blocks, & top-level
- Experience with full-chip IR-drop sign-off with industry standard tools a must
- Knowledge of 28nm, 16nm technology is required
- Exposure to 10nm and below challenges is a plus
- Ability to script in the Cadence and/or Synopsys environments is required
- Must be able to code and maintain TCL, PERL scripts
- Knowledge of CPF/UPF flows and low-power methodology

56 Senior Physical Design Engineer

Resume Examples & Samples

- Running/supporting/maintaining the PnR Flow using industry standard EDA tools for designing the next generation Multi-Ghz high-performance processor SOC chips in leading-edge CMOS process technology

- Work with design teams across various disciplines such as Digital/RTL/Analog in helping them take their blocks (custom, PnR) through the physical design flow and making sure all the blocks meet timing requirements
- Work with physical verification team to integrate these blocks seamlessly into full chip partitions
- Provide technical direction, coaching, and mentoring to employees on the team and others when necessary to achieve successful project outcomes
- Writing scripts in TCL and Perl to achieve productivity enhancements through automation is required
- Diligent, detail-oriented, and handles assignments with minimal supervision
- Self-driven individual and a good team player
- Ability to interface internally and externally with other departments
- Grounded, detail-oriented

57 Asic Physical Design Engineer

Resume Examples & Samples

- 5+ years IC design experience
- Experience with ASIC physical design using automated synthesis, placement, routing and verification tools
- Ability to understand advanced digital design architectures and clocking structures to help manage timing and physical design constraints
- Ability to work with digital and analog circuit designers to analyze and explore physical implementation options for complex designs integrating standard cell logic with high speed custom interface circuits
- Experience using static timing, signal integrity and power analysis tools using a standard cell design flow
- DRC/LVS verification experience with full chip layouts using physical verification tools
- Familiarity with Cadence Encounter tools is an asset
- Experience with physical design methodologies and TCL scripting is required
- Experience with low power design flows at advanced process nodes is a benefit
- Previous digital design and RTL coding experience a plus
- Strong communication skills, with the ability to convey complex technical concepts to other design peers in verbal and written form
- A high level of self-motivation and the ability to be a self-starter

58 Lead Physical Design Engineer

Resume Examples & Samples

- Running/supporting/maintaining the Global Assembly Flow using industry standard EDA tools for designing the next generation Multi-Ghz high-performance processor SOC chips in leading-edge CMOS process technology
- Work with design teams across various disciplines such as Digital/RTL/Analog in helping them take their blocks (custom, PnR) through the global Assembly flow and making sure all the blocks meet physical requirements
- Implement/Support blocks with multi-voltage designs through all aspects of RTL to GDS Implementation (Place and Route, static timing, physical verification) using industry standard EDA tools
- Work with physical block owners in integrating blocks seamlessly into full chip partitions
- Good analysis and problem-solving skills
- Initiative and a bias for thoughtful action
- Diligent, detail-oriented, and handle assignments with minimal supervision

59 Physical Design Engineer

Resume Examples & Samples

- Address various physical issues
- Successfully close several digital blocks
- Support/enhance the Place & Route Flow using industry standard EDA tools
- Work with the RTL team in moving their blocks (coded in Verilog) through the Place & Route Flow
- Generate back end views that meet timing requirements
- Work with physical verification team to integrate these blocks with minimal issues
- A significant amount of tool customization is required for our semi-custom and full-custom design environments
- Provide technical direction, coaching, and mentoring to employees on your team and others when necessary to achieve successful project outcomes
- Must demonstrate initiative and a bias for thoughtful action
- Grounded, detail-oriented, always backs up ideas with facts

60 Asic Physical Design Engineer

Resume Examples & Samples

- 2) Experience in working on large scale chip top level layout is a plus
- 3) Ability to understand STA and timing constraints
- 4) Ability to work with designer to analyze and optimize layout for timing critical analysis
- 5) Ability to work independently and reach development milestones under an aggressive schedule

is very important

61 ~~Principal Physical Design Engineer~~

Resume Examples & Samples

- Floorplanning including multi-power domain, PG planning etc
- Physical implementation of blocks and top-level including clock-tree
- Physical verification and timing closure for block and chip-level
- Static and dynamic IR drop analysis, signal and power EM checks
- ·Methodology & Flow development of Physical Design and Timing Closure
- Interfacing with internal and external teams including Design, IP, Library

62 Physical Design Engineer

Resume Examples & Samples

- Physical design flow from synthesis, static timing closure, formal verification, floor planning, CTS, placement, route, post route optimization, extraction, physical verification, and ECO flow
- Place and route tools: Cadence SOC Encounter, Synopsys ICC
- Taping out chips at 65nm or below

63 Physical Design Engineer

Resume Examples & Samples

- Backend Flow put in place know-how
- Cadence Backend Suite, Innovus
- Multi-Mode Multi-Corner use
- Parasitic extraction
- Scripting in Python, Perl, TCL
- Expert in problem solving with numerous tools
- Master degree (Electrical engineering) or similar
- Minimum 2 years of experience in physical design IC
- Good knowledge in global backend flow
- Knowledge in synthesis, equivalence checking and power analysis is a plus
- Drive the methodology definition and maintenance over time
- Have good technical coordination skills to interact with all designers and layout team

- Flexibility to parallelize tasks as the position is central
- Have excellent English skills (oral and written)
- Strong interpersonal skills in international environment

64 Analog Physical Design Engineer

Resume Examples & Samples

- Have worked until now with: Analog Physical design (IC layout) , DDFX, physical design verification , CADENCE, Virtuoso, First encounter, CMOS process
- Have good configuration management skills
- Have good technical English skills
- Contract will be limited for one year, because it is a maternity leave replacement. But an extension is possible

65 Physical Design Engineer

Resume Examples & Samples

- Work as a member of the physical design team to implement digital subsystems for mixed signal IC’s
- Support all phases of the Place and Route flow including
- A B.Sc. degree in Electrical or Computer Engineering
- An understanding of timing driven place and route flow
- An understanding of Static Timing Analysis and timing closure is preferred
- Knowledge and/or experience with implementation EDA tools preferred (i.e. Synthesis, STA, Formal Verification Power Analysis) is preferred
- Strong scripting and/or programming skills
- Experience with related programming/scripting languages e.g. TCL, Perl, and C
- Working knowledge of PC and Unix/Linux operating systems
- Enjoys working a team environment
- Well organized, and detail oriented

66 Senior Asic Physical Design Engineer

Resume Examples & Samples

- At least 7 years of industry experience in ASIC/SoC Design and IP Integration

- Defining timing constraints/exceptions, updating timing budgets
- Synthesis using Synopsys Design Compiler
- Place and Route using IC Compiler: floorplanning, placement, custom clock tree synthesis, routing and block finishing
- Timing closure (PrimeTime)
- Signoff checks: LEC/ATPG/LVS/DRC/ANT. Power and noise analysis. Place and Route flow enhancements in TCL/Perl
- Low Power Implementation based on UPF (automatic grid synthesis, level shifters & isolation cells insertion),
- Knowledge of the flow up to 28 nm
- In addition, Synthesis and place and route done via Synopsys LYNX cockpit is a real plus
- PERL, Python
- Perform RTL to GDSII flow for a complete chip

67 Physical Design Engineer SD

Resume Examples & Samples

- Bs.c in electrical engineering or equivalent
- 4-6 years in physical design implementation including synthesis, floor plan, clock tree synthesis, routing, timing optimization, LVS and DRC
- Knowledge of synopsys implementation tools DC,ICC and verification tool advantage
- Knowledge of scripting and scripting capabilities an advantage

68 Physical Design Engineer

Resume Examples & Samples

- Motivation to drive an exciting project
- Experience solving SoC issues such as ESD strategies, mixed signal block integration, and package interactions
- Familiar with hierarchical design approach, top-down design, area budgeting and physical verification convergence
- Experience with large SoC designs (>20M gates) with frequencies in excess of 1GHz utilizing 16nm and more advanced technologies
- From a CAD tool perspective, experience with floorplanning tools, P&R flows and physical design verification flows is required
- Familiar with various process related design issues including Design for Yield and Manufacturability, multi-Vt strategies and thermal management

- TCL and Bash mastery are a necessity; Make, Perl and Python expertise is nice to have

69 Physical Design Engineer

Resume Examples & Samples

- BSEE in Electrical or Computer Engineering
- Experience with designs that contain high amounts of analog and digital content
- Experience with block and top-level design using the Cadence APAR tool suite
- Experience with hierarchical design using the Cadence APAR tool suite
- Experience with Mentor Calibre verification tool suite
- Experience with StarRC extraction, QRC extraction, PrimeTime SI, and Celtic tools
- Skills using TCL, PERL, and Make scripting
- Data processing and manipulation skills using sed, awk, grep, emacs
- Strong Unix/Linux background
- Good writing and publishing skills to release documentation and train other users
- Good communication skills as well as a strong willingness to learn from more experienced engineers
- Excellent written and verbal communication skills with a track record of excellent customer support
- Self-motivated with the ability to work independently and interface effectively with team members in a remote location

70 Big Core Physical Design Engineer

Resume Examples & Samples

- Work experience with VLSI circuit design
- Strong knowledge of synthesis
- Experience with Static timing analysis skill
- Optimize the floorplan and metal routing for design blocks

71 Big Core Senior Physical Design Engineer

Resume Examples & Samples

- Willingness to work with others in a highly complex decision space rife with ambiguity
- Ability to develop an implementation plan, monitor key indicators, and adjust resources and scope

to deliver value on schedule

- Strong verbal and written communication and collaboration skills
- Candidate must have a Technical Electrical/Computer Engineering Bachelor's degree in Electrical Engineering or Computer Engineering with 10+ years of design experience or a Master's degree in Electrical Engineering or Computer engineering with at 8 least years of experience in technical design
- Knowledge in RTL, VLSI circuit design, synthesis, floor planning, layout, static timing analysis, low power optimization, and quality checks
- Experience in CPU is preferred
- Experience with UNIX, Perl and TCL is also desired

72 Senior Physical Design Engineer

Resume Examples & Samples

- You will be responsible for implementation of all phases of ASIC/SOC design (RTL2GDSII flow)
- RTL synthesis and APR using industry standard tools
- Driving power, timing, and layout convergence of multiple designs
- Digital Back-end physical design
- Debugging post-silicon circuits and systems to root-cause logic and circuit issues
- Bachelor of Science Degree in Computer Engineer, Electrical Engineering or equivalent
- 10+ years of work experience
- Previous work experience with DFT Scan Insertion and ATPG vector generation
- Previous work experience with Synthesis tools, Floorplanning tools, P&R flows, global timing verification and Physical Design Verification Flows is required
- Work with physical design team, drive methodologies and “best known methods” to streamline physical design work, come up with guidelines and checklists, drive execution, and track progress
- Hands on experience in Synthesis, physical design, backend timing and large chip integration
- Experience with DFT Scan Insertion and ATPG vector generation
- Familiarity with all aspects of ASIC integration including Floorplanning, Clock and Power distribution, global signal planning, I/O planning and hard IP integration (Digital / RF / Mixed Signal)
- Familiarity with typical SoC issues such as multiple voltage and clock domains, ESD strategies, mixed signal block integration, and package interactions
- Familiarity with hierarchical design approach, top-down design, budgeting, timing and physical convergence
- Experience with large SoC designs (>20M gates) utilizing state of the art deep sub-micron technologies
- Detailed understanding of database management issues

- Work with external ASIC Vendors to drive SOC execution forward
- Be focal point for place and route drive the work among place and route engineers, set goals and milestones, plan short and long-term work, understand dependencies between different domains like top, STA, block place and route
- Resolve design and flow issues related to physical design, identify potential solutions and drive execution

73 Physical Design Engineer

Resume Examples & Samples

- Full-chip Static Timing Analysis, timing constraints generation and debug, and timing convergence of large scaled SoCs required
- Physical design aspect of timing closure and closing timing by improving placement, routing, cell sizing, buffering, logic optimization, etc. needed
- Analyzing and converging on crosstalk delay, noise glitch, and electrical rules in deep-sub micron processes required
- Process variation effects and modeling techniques - Timing models - Scripting language, such as, Perl, Tcl, Unix Shell
- Statistical timing analysis preferred - Methodology or flow development/automation - Good verbal and written communication skills - Ability to work in a team environment - Organized and motivated

74 Physical Design Engineer

Resume Examples & Samples

- Must have experience in completing PD tasks on recent Technologies
- Needs clocking architecture knowledge
- Will work directly with Timing Team to ensure Design closure
- Bachelor’s in Electrical Engineering plus 8 or more years of experience
- Master’s Degree in Electrical Engineering
- Experience working with communications chips

75 Physical Design Engineer

Resume Examples & Samples

- Analog full custom layout of RF / Mixed-Signal blocks and macros in deep- submicron CMOS technologies - Floor planning of layout blocks and macros

- Analog and ESD Layout
- Schematic to layout verification of analog blocks and macros DRC/LVS/ERC
- Identify areas of methodology improvements within the Physical Design development with respect to quality, throughput and reusability

76 Asic Physical Design Engineer

Resume Examples & Samples

- Bachelor's degree in Electrical Engineering or a related discipline and a minimum of 5 years of relevant experience (3+ years with an MS, 0 years with a PhD.)
- Experience in full product life cycle of ASIC Design
- Experience in backend ASIC design including synthesis and static timing analysis, place and route, physical verification (LVS/DRC)
- Experience with Cadence ASIC toolset e.g., Innovus, Genus, Tempus etc
- Proficiency in HDL (VHDL/Verilog)
- Proficiency in scripting languages such as Tcl, Python or Perl
- U.S. citizenship with the ability to obtain and maintain a Secret security clearance
- Effective communication and presentation skills and high proficiency in technical problem solving
- Master's Degree in Electrical or Computer Engineering
- Experience with advanced technology nodes (sub 20nm)
- Experience with Global foundries, TSMC or Honeywell Foundries
- Knowledge of DFT, scan insertion and ATPG is a plus
- Active DoD Secret Clearance or higher

77 Senior Physical Design Engineer

Resume Examples & Samples

- Minimum of 5 years of industry related experience
- Familiarity with industry standard Physical design flows is a must
- Must have experience in power grid design, estimating power, verifying IR-drop, noise, checking DRC, LVS, at block and chip level
- Must be able to place & route hierarchical blocks
- Require experience IR-drop/EM, power, noise sign-off with industry standard tools
- Knowledge of CPF/UPF flows and low-power methodology is a must
- Previous experience in high performance ARM cores is a plus

Emerging Memory Physical Design Engineer

- Must have strong skills in custom layout, floor planning, matching techniques and manual routing
- Be able to learn and understand design rules and deliver quality layout
- Understanding of layout methodology from initial chip plan to tapeout
- Strong debug and problem-solving skills for LVS, DRC and layout issues without much supervision
- Experience with Cadence tool, VXL, Calibre tool
- Independent with strong analytical skills, creative thinking and self-motivated
- The position requires an individual with the ability to learn rapidly and adapt quickly to changing situations
- Layout experience with memory array is plus
- Experience coordinating and supervising the work of others
- Experience in layout design on non-volatile memory
- Familiarity with CAD and EDA tools including Cadence Virtuoso, Calibre & Hercules
- Knowledge of programming languages like Perl, Skill and Shell scripting

79 Physical Design Engineer

Resume Examples & Samples

- Will be responsible for all aspects of Physical Design for Fullchip/Blocks covering Floorplanning, Budgeting, Clock Tree planning & analysis, Placement, Scan re-ordering, Clock tree synthesis, Placement optimizations, Routing, Timing and SI analysis/closure, ECO tasks (both timing and functional), EM/IR, DRC, LVS, ERC analysis & fixes, Low Power solution development & implementation
- Prefer sound knowledge in EDA tools such as DC, ICC2, Cadence Innovus, STAR-RC, PT-SI, Verplex, Quartz, Calibre, internal tools & flow, etc
- Work closely with the design team throughout the project life cycle to debug issues & implement the physical design in the most efficient way to save Power, Area & achieve High performance
- Work closely with the methodology team to solve the implementation challenges & provide inputs to improve the Physical design flow
- Experienced in design automation
- Understanding of Timing constraints, SI prevention, Power reduction
- Must have prior experience with Synopsys/Cadence/Mentor place and route tools
- Must have completed design in 28nm and/or 16nm
- Proficient in Unix/TCL/Perl
- Good communication and presentation skills. Requires good interpersonal skills and problem-

solving ability

80 Senior Physical Design Engineer

Resume Examples & Samples

- Floor-planning, Place & Route and CTS using physical design tools
- Physical verification and IP Integration
- Physical Design Flow and Methodology
- Ability to lead the team along with the project execution
- Use metric-driven techniques to help ensure first-pass working silicon
- Communicate regularly with the implementation and project team to resolve issues, and communicate status to leads
- Occasional travel needed
- Expertise in Physical Design activities: Floor-planning, CTS, P&R, Extraction, Power IR/EM, Physical Verification (DRC/LVS) and Signal Integrity
- Static Timing/Crosstalk Analysis and timing closure
- Must have an understanding of Synthesis/DFT concepts and flow
- Experience in working with analog IP, hard and soft macros and delivering hierarchical design projects
- Expertise with Backend Tools (Innovus or ICC, PVS, Tempus, Voltus, QRC)
- Strong programming knowledge in Perl, TCL, and/or Shell and Python Scripting
- Excellent oral and written communications skills in order to work with teams across the globe

81 Principal Physical Design Engineer

Resume Examples & Samples

- Perform custom RF Physical Design, including block-level and top level layouts, floorplanning, package routing, etc
- Work with designers to optimize block area, iterate critical layouts for parasitic improvement, and properly route sensitive nets
- Conform to overall chip layout methodology
- 5 years of experience in RF or Analog physical design flows and methodologies in deep submicron CMOS (65nm and below)
- Experience with ASIC physical design, including LVS/DRC/PEX verification and debug
- BS degree in Electrical Engineering
- 10+ years in RF Layout (LNA, Mixer, PA, VCO, High Frequency ADC and DAC)

Senior Physical Design Engineer

Resume Examples & Samples

- Knowledge about industry standards and practices in Physical Design, including Physically aware synthesis, Floor-planning, and Place & Route
- Solid Understanding of all aspects of Physical construction, Integration and Physical Verification
- Working Knowledge of Basic SoC Architecture and HDL languages like Verilog to be able with logic design team for timing fixes

83 Physical Design Engineer

Resume Examples & Samples

- Master of Science in Electrical Engineering or related discipline
- 2+ years' experience with RTL synthesis
- 2+ years' experience using Place&Route tools
- 2+ years' experience with CPU and GFx core hardening
- Should have experience working with a team trying to hit performance, power, and area targets
- Excellent problem solver

84 Physical Design Engineer

Resume Examples & Samples

- Required: Bachelor's, Computer and/or Electrical Engineering, Preferred: Master's, Computer and/or Electrical Engineering
- 8+ years experience
- Knowledge of power intent formats (CPF/UPF) a plus

85 Physical Design Engineer Graduate Intern

Resume Examples & Samples

- The candidate must be pursuing a Master's Degree in Electrical Engineering, Computer Engineering, Computer Science, Hardware Engineering or other related field of study
- 6+ months of experience working in/with
- Memory custom layout is a preferred qualification
- Custom layout floor planning, RC extraction, layout optimization and verification

- ESD, lithography, EM, DFM, antenna effects and manufacturing challenges
- UNIX with experience in scripting and debugging
- VLSI circuits, design techniques, and sub-micron CMOS technologies
- Designing high-speed, analog circuits, floor planning, timing convergence, physical design convergence, formal equivalency verification, device layout, and design rule checking
- Logic synthesis and automated place and route tools
- Hardware description languages such as Verilog or System Verilog

86 Lead Physical Design Engineer

Resume Examples & Samples

- Implementation of physical design for large high speed chips in deep submicron process
- Responsible to meet block goals for timing, area, and design rules, and will own multiple design blocks within a chip from initial RTL to tape out
- Leading and mentoring junior employees and interfacing with front end design team to improve RTL and design quality
- Ability to define problems, issues and opportunities, analyze data, establish facts, and draw valid conclusions from various datasets

87 Structural / Physical Design Engineer

Resume Examples & Samples

- Define VLSI structural design methodologies and develop design flows
- Implement structural physical designs and integration
- Verify structural physical designs for, such as functional equivalency, timing/performance, noise, layout design rules, reliability and power
- Oversees definition, design, verification, and documentation for an IP/Subsystem/SoC development
- Determines architecture design, logic design, and system simulation
- Contributes to the development of multidimensional designs involving the layout of complex integrated circuits

88 Senior Principal Physical Design Engineer

Resume Examples & Samples

- Block and SoC level floorplanning

- RTL systhesis
- Timing constraints
- Power grid analysis
- Chip floor planning
- Clock distribution and CTS
- Parasitic Extraction
- Timing driven place and route
- Logical Equivalency Checking (LEC)
- Static timing analysis, timing closure, signal integrity
- LVS and DRC
- Development of design methodologies and enhancements of existing EDA techniques
- Debug/analysis skills for library and technology files
- Team oriented, with strong communications skills
- Knowledge of power intent formats (CPF/UPF)

89 Physical Design Engineer

Resume Examples & Samples

- PhD or MS in CS, EE related field
- Familiar with design rule, CAD/algorithm, APR/chip implementation, and/or chip integration
- English writing & communication

90 Physical Design Engineer / Technical Manager

Resume Examples & Samples

- Design and Process co-optimization for advanced technology
- EDA enablement and design methodology development
- Chip integration
- Innovative in problem solving and design solution development
- PhD or MS in CS or EE related field

91 Principle Physical Design Engineer

Resume Examples & Samples

- PD skill at both RLM and Top Level experience required
- Clocking skills (knowledge of Physical Routing tools plus Timing implications)
- Bachelor’s in Electrical Engineering plus 11 or more years of experience

92 Senior Physical Design Engineer

Resume Examples & Samples

- Self-Starter with atleast 8+ years of relevant experience in the semiconductors industry (Physical Design)
- Bring in some unique expertise
- Power Grid , Static IR , Dynamic IR analysis
- Power Integrity / Signal Integrity
- Power & Signal EM Analysis

93 Physical Design Engineer CG

Resume Examples & Samples

- Build and verify all levels of physical design hierarchy leaf cell, IP block, and compiler
- Adept problem solver with a disciplined approach to problem solving
- A team player willing to share knowledge
- A self-starter proactively seeking solutions
- Flexible and able to multi-task
- Master's Degree in Electrical Engineering, Computer Engineering or Computer Science

94 Physical Design Engineer

Resume Examples & Samples

- You should hold a Bachelor's/Master's degree in Electronic Engineering or equivalent with about 3 years relevant experience including a solid educational background in IC design
- Experience with physical design or RTL2GDS methodologies is not necessarily required, but would be an advantage
- A strong demonstrated commitment to teamwork
- Hands on experience with UNIX/Linux environments and scripting languages such as Tcl/Perl would be beneficial

Senior Physical Design Engineer

- Expertise in Physical Design activities: Floor-planning, CTS, P&R, Extraction, IR drop analysis, STA, Physical Verification and Signal Integrity
- Expertise with Physical Design tools (Innovus or ICC)
- Experience with tools and methodologies for P & R -- placement checks, clock gating timing, logic restructuring, and optimization
- Experience in closing timing on block level
- Strong programming knowledge in Perl, TCL, and/or Shell Scripting
- Must be able to work autonomously

96 Lead Physical Design Engineer

Resume Examples & Samples

- Physical design implementation utilizing recent technologies (7/14/16nm preferred but 28nm/32nm acceptable) in the following areas: Top-level integration, floorplanning, placement and routing, clocking, and timing closure, and physical design verification (PDV)
- Knowledge of digital VLSI design, methodology, and process
- Experience with tools from Cadence or Synopsys for digital implementation
- 8 years minimum industry-related experience
- Travel – less than 5%
- Fluent in English Language – written & verbal
- Ability to use scripting languages to automate process flow
- Effective communicator to provide status of the progress, problem and solution to management and other engineers

97 Physical Design Engineer

Resume Examples & Samples

- Candidate must have a Master's Degree of Science in Electrical or Computer Engineering or any related discipline
- C/C++, Perl, TCL, Shell scripting
- Placement and routing CAD tools

Senior Physical Design Engineer

Resume Examples & Samples

- Engagement and collaboration across functional teams is a key aspect of this role
- Strong ability to clearly articulate a defects root-cause and provide recommendations to systematically address the problem is needed
- Capable to interface with customer is desired
- Timing and enhancement of static timing environment
- Debugging failures in all areas of physical and circuit design
- Ability to implement ECOs
- Methodology experience a strong plus
- Understanding of synthesis, logic mapping
- Understanding of clock and reset domain crossing strategies and effects
- Understanding of timing constraints creation
- Understanding of Power grid analysis and IR drop
- Ability to run and fully understand Logical Equivalency Checking (LEC)
- Understanding of and ability to run static timing analysis, extraction, signal integrity
- Understanding and ability to run LVS and DRC
- Understanding of package and die interactions on system level solutions
- Applicant should have excecllent debugging and logic design skills
- Sub-micron CMOS circuit and technology issues
- Excellent Debug, analysis skills
- Knowledge in other areas of chip design a strong plus

99

Physical Design Engineer

Resume Examples & Samples

- Designs, implements, and verifies layout of reliability test structures and circuits
- Executes and debugs layout automation design flows
- Evaluates and characterizes layout design properties
- Modifies physical designs to comply with latest manufacturing guidelines and engineering changes. Develops solutions to problems utilizing formal education and judgment
- Documents specifications and methodologies used for physical design
- Ability to interact effectively with engineers from various disciplines and communicate effectively with technical leads and peers
- Self-motivated with the initiative to seek constant improvements in physical design methodologies

- Possess strong initiative, analytical/problem solving skills, team working skills, ability to multitask and be able to work within a diverse team environment
- Attention to details and discipline in following defined methodologies
- The candidate must possess a MS in Electrical Engineering or Computer Engineering
- Knowledge of CMOS VLSI Design concepts, flows, and EDA tools
- Experience with Cadence Virtuoso Layout Suite
- Experience debugging layout verification flows e.g. DRC, LVS, RVExperience with UNIX/Linux environments and scripting languages e.g. PERL or TCLExperience with Cadence SKILL Programming language

100 Physical Design Engineer

Resume Examples & Samples

- Self-Starter with atleast 5+ years of relevant experience in the semiconductors industry (Physical Design)
- Exposure to Analog and Digital Integration Rules as well as analog tools is a plus
- Be fluent with physical design Concepts and Tools
- Drive technological innovations in the team
- Mixed Signal Design , noise analysis
- Critial Path circuit analysis

101 Physical Design Engineer

Resume Examples & Samples

- Knowledge of MCAD, Pro-E, CREO2
- Knowledge of Telcordia and/or military, IPC and ASME standards
- Able to run small mini projects with minimal supervision

102 Senior Physical Design Engineer

Resume Examples & Samples

- Physical design implementation from netlist to gdsii, on advanced nodes, 16nm and below
- Floorplanning and design optimization for speed/area/power
- Integration of in-house and 3rd party digital/mixed-signal/analog IP
- Physical design closure, including DRC/LVS/ANT

- Static timing analysis, debug and timing closure/signoff
- Flow development to avail of latest enhancements in implementation tools
- Supervision and mentoring of junior engineers
- 10+ year relevant experience
- Expert knowledge of P&R implementation, physical verification and STA tools
- Full chip implementation on advanced finfet nodes 16nm and below, utilizing double/triple pattern technologies, and multi-million instance block level designs
- Mutivoltage design flows, familiarity with UPF/CPF, IR drop analysis
- Excellent debugging and problem solving skills
- Exposure to latest P&R implementation tools (e.g. ICC2/Innovus) a plus
- Flip chip implementation, including custom and automated RDL routing
- Familiarity with AREA-IO, LUP and ESD prevention / resolution
- Prior experience integrating hard IP such as USB, PCIE, DDR, MIPI etc

103 Physical Design Engineer CG

Resume Examples & Samples

- Bachelor's or Master’s Degree in Electrical Engineering, Computer Engineering, Computer Science or Technical educational background
- Previous experience in Physical Design is a plus
- Proficient Programming skills UNIX shell script, Tcl, Perl

104 Physical Design Engineer

Resume Examples & Samples

- Minimum 5 years experience in physical design of advanced mixed signal circuits like voltage regulators, DC-DC converters, Bandgap, Data convertors etc
- Proven mixed signal layout skills with multiple tapeouts
- Good understanding of MOS Device physics and process is a must
- A working knowledge of ESD, latchup and matching is highly desirable
- Experience with layout tools like Virtuoso XL, calibre, Virtuoso custom place and route is preferred
- Multiple technology nodes and HV layout experience a big plus
- Zero defects and DfX mindset from the start

- Experienced physical design engineer (5+ years) with strong STA background
- High level of expertise with Synopsys Primetime and ability to write timing ECOs in ICC is required
- Expert in writing timing constraints and analyze block level design and suggest design modifications to achieve timing closure
- Strong scripting skills are desirable (TCL and Perl)
- Experienced with all aspects of physical design
- Must have gone through at least one tape-out of a large, high speed design (?50 M instances)Search Jobs US

106 Physical Design Engineer

Resume Examples & Samples

- Experience with physical design implementation in recent technologies (7/14/16nm preferred but 28nm/32nm acceptable) in the following areas: Top-level integration, floorplanning, placement and routing, clocking, and timing closure, and physical design verification (PDV)
- Work effectively with global team and be self-motivated to solve problems and manage deliverables
- Education – BS in Electrical Engineering or Computer Engineering
- Experience – 8 years minimum industry-related experience
- Experience with Cadence or Synopsys tools

107 Asic Physical Design Engineer

Resume Examples & Samples

- Excellent understanding of ASIC design methodologies from netlist to GDS
- Familiar with all aspects of physical implementation including Floor planning, Clock and Power distribution, global signal planning, I/O planning
- Familiar with hierarchical design approach, top-down design, budgeting, timing constraints and physical convergence
- Hands on experience in block level implementation including physical synthesis, placement, routing and optimization with Innovus/ICC2 primetime and timing closure
- Familiarity with low power design and custom placement implementation
- Experience with large designs utilizing state of the art sub 16/14 nm technologies

- Strong communication skills and ability to work as a team player
- Floor planning and P&R tools: Cadence Innovus & Synopsys ICC2
- Synthesis Tools: Synopsys DC/DCG; Cadence Genus
- Formal Verification : Synopsys Formality and Cadence LEC
- Static Timing verification (Primetime/PTPX)
- Familiarity with Physical Design Verification Flows is a plus
- Scripting: TCL, Perl is required; Python is a plus

108 Physical Design Engineer

Resume Examples & Samples

- Work with our front-end design and physical design teams to develop leading-edge physical implementations and silicon products
- Expand your in-depth understanding and experience with physical design tools and flows – from RTL to GDS
- Your work will focus on the full development flow: Floor planning, Bus / Pin Planning, Clock Tree Synthesis, Placement, Optimization, Routing, Parasitic Extraction, Static Timing Analysis, IR drop analysis, Physical Verification and Sign Off
- Be a highly-valued member of our start-up like team through excellent collaboration and teamwork with other physical design engineers as well as with the RTL design team
- Flow development, Innovation, optimization and scripting
- 10+ years of experience as a physical design engineer with expertise in RTL-to-GDSII flow, floor planning, Clock tree synthesis and block-level/chip-level signoff
- Successfully complete several product development cycles
- Strong communication, time management and technical skills
- Expertise using leading-edge EDA tools (Synopsys, Cadence or Mentor Graphics)
- Experience in integrating IP from both internal and external vendors and be able to specify and drive IP requirements in the physical domain
- Ability to plan, execute, course correct and optimize blocks and SoC level implementations

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